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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,909	03/26/2004	Dong-Ho Park	4591-377	5051
20575	7590 12/29/20	5	EXAM	IINER
	OHNSON & MCC	TRAN, MICHAEL THANH		
210 SW MORRISON STREET, SUITE 400 PORTLAND, OR 97204			ART UNIT	PAPER NUMBER
•			2027	

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)			
	10/813,909	PARK ET AL.			
Office Action Summary	Examiner	Art Unit			
•	Michael t. Tran	2827			
The MAILING DATE of this communication	on appears on the cover sheet with	the correspondence address			
Period for Reply					
A SHORTENED STATUTORY PERIOD FOR F WHICHEVER IS LONGER, FROM THE MAILII  - Extensions of time may be available under the provisions of 37 of after SIX (6) MONTHS from the mailing date of this communicate.  - If NO period for reply is specified above, the maximum statutory.  - Failure to reply within the set or extended period for reply will, by Any reply received by the Office later than three months after the earned patent term adjustment. See 37 CFR 1.704(b).	NG DATE OF THIS COMMUNICA CFR 1.136(a). In no event, however, may a repli ion. period will apply and will expire SIX (6) MONTH statute, cause the application to become ABAN	ATION.  y be timely filed  S from the mailing date of this communication.  IDONED (35 U.S.C. § 133).			
Status					
1) Responsive to communication(s) filed on	24 October 2005.				
2a)⊠ This action is <b>FINAL</b> . 2b)□	This action is FINAL. 2b) This action is non-final.				
•	] Since this application is in condition for allowance except for formal matters, prosecution as to the merits is				
closed in accordance with the practice ur	nder <i>Ex parte Quayle</i> , 1935 C.D. 1	1, 453 O.G. 213.			
Disposition of Claims					
4) ⊠ Claim(s) <u>1-22</u> is/are pending in the application 4a) Of the above claim(s) is/are with 5) ⊠ Claim(s) <u>7-22</u> is/are allowed.  6) ⊠ Claim(s) <u>1,3 and 4</u> is/are rejected.  7) ⊠ Claim(s) <u>2,5 and 6</u> is/are objected to.  8) □ Claim(s) are subject to restriction	thdrawn from consideration.	<i>,</i>			
Application Papers					
9) The specification is objected to by the Example 10) The drawing(s) filed on is/are: a) Applicant may not request that any objection Replacement drawing sheet(s) including the control of the oath or declaration is objected to by the control of the oath or declaration is objected.	☐ accepted or b)☐ objected to by to the drawing(s) be held in abeyance correction is required if the drawing(s)	e. See 37 CFR 1.85(a). is objected to. See 37 CFR 1.121(d).			
Priority under 35 U.S.C. § 119  12) Acknowledgment is made of a claim for for a) All b) Some * c) None of:  1. Certified copies of the priority docu 2. Certified copies of the priority docu 3. Copies of the certified copies of the application from the International E * See the attached detailed Office action for	uments have been received. uments have been received in App e priority documents have been re Bureau (PCT Rule 17.2(a)).	olication No eceived in this National Stage			
		WTW			
Attachment(s)  1) Notice of References Cited (PTO-892)  2) Notice of Draftsperson's Patent Drawing Review (PTO-9  3) Information Disclosure Statement(s) (PTO-1449 or PTO/Paper No(s)/Mail Date	48) Paper No(s)/l	rmal Patent Application (PTO-152)			

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#### DETAILED ACTION

1. In response to the Communications dated October 24, 2005, claims 1-22 are active in this application.

### Claim Objections

2. Claims 2, 5, and 6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### Claim Rejections - 35 U.S.C. § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- (e) the invention was described in-
- (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
- (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

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4. Claims 1, 3 and 4 are rejected under 35 U.S.C 102(b) as being anticipated by Kwon et al. [U.S. Patent #5,768,215].

With respect to claim 1, Kwon et al. disclose, in figures 5, 6, and 11b, a semiconductor memory device comprising: a plurality of first bit lines [1A], a plurality of second bit lines [1B]; a signal generator circuit [2] structured to produce a flag signal [Rop] notifying a burst [page] read operation; an address generator circuit [12] structured to provide an address in response to the flag signal; a column selection circuit [13] structured to select a part of the plurality of first bit lines in response to the addresses, and connect [via elements 12b and 15b - see figure 6] the first bit lines to the plurality of second bit lines [via st], respectively; and a discharge circuit [3] for discharging [via phi.DCB] voltages from the plurality of second bit lines in response to the flag signal [see figure 11b]. In figure 11b, it is noted that phi.DCB is responsive to signal Rop. It is noted that the connection of the first bit lines to the plurality of second bit lines are being interpreted in two ways: 1) by the column selection circuit via elements 12b and 15b, which is shown above; and 2) by the combination of the column selection circuit with elements 12b and 15b being treated as one single circuit which still has the functionality of the column selection circuit. In both interpretations, the first bit lines and the plurality of second bit lines are made to connect to one another. Also, see column 7, lines 35-40. In the cited section, Kwon et al. clearly indicates that the column selection circuit couples both the first and second plural bit lines.

With respect to claim 3, Kwon et al. disclose, in column 2, that the signal generator circuit is structured to produce the flag signal synchronized to a clock signal.

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With respect to claim 4, Kwon et al. disclose, in column 1, that the device is applicable to a flash memory.

#### Remarks

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. See above explanations regarding the amended claim 1.

Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for response to this final action is set to expire THREE MONTHS from the date of this action. In the event a first response is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the statutory period for response expire later than SIX MONTHS from the date of this final action.

## Allowable Subject Matter

- 6. Claims 7-22 are allowable over the prior art of record.
- 7. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

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 A signal generator circuit structured to produce the flag signal notifying a next burst read operation after an input of an initial address.

- A discharge circuit comprises: a discharge signal generator structured to
  produce a discharge signal in response to the flag signal; and a plurality of
  NMOS transistors respectively connected between the plurality of second bit
  lines and a ground voltage and controlled by the discharge signal.
- The second bitlines are structured to be discharged before the selecting operation of the column selection circuit.
- A signal generator circuit for generating a flag signal indicating a burst read
  operation in response to a clock signal and a chip enable signal; and a sense
  amplification circuit for sensing and amplifying voltages of the selected
  second bit lines in response to the sense amplification control signals during
  the burst read operation.
- A discharge circuit for discharging voltages of the plurality of second bit lines in response to the flag signal.
- After the global bit lines are discharged, selecting the local bit lines and the global bit lines in response to the address.
- Sensing the cells located at the new address using the previously discharged one or more bit lines.

#### Conclusion

8. When responding to the Office action, Applicants are advised to provide the

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Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

9. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

10. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-1650.

Michael T. Tran Art Unit 2827 December 21, 2005

MICHAEL TRAN PRIMARY EXAMINER